



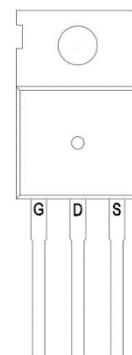
SSC8LA12GT4

N-Channel Enhancement Mode MOSFET

➤ Features

V _{DS}	V _{GS}	R _{DS(ON)}	I _D
100V	±20V	3.7mΩ@10V	150A
		4.9mΩ@4V5	

➤ Pin Configuration



TO-220-3L (Top View)

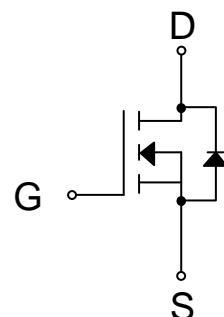
➤ Description

This device is N-Channel enhancement MOSFET. Uses SGT technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit.

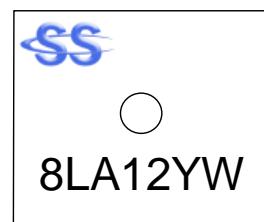
100% UIS + ΔVDS + R_g Tested!

➤ Applications

- Motor Drive Control
- Portable Devices
- DCDC Conversion
- Power Supplies
- Synchronous Rectification



Pin Configuration



Marking

(YW: Internal Traceability Code)

➤ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GSS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current ^d	$T_C=25^\circ\text{C}$	150
		$T_C=100^\circ\text{C}$	69
I_{DSM}	Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	26
		$T_A=70^\circ\text{C}$	19
I_{DM}	Pulsed Drain Current ^b	450	A
P_D	Power Dissipation ^c	$T_C=25^\circ\text{C}$	96
		$T_C=100^\circ\text{C}$	38
P_{DSM}	Power Dissipation ^a	$T_A=25^\circ\text{C}$	4.2
		$T_A=70^\circ\text{C}$	2.7
I_{AS}	Avalanche Current ^b L=0.5mH Single Pulse	45	A
E_{AS}	Avalanche Energy ^b L=0.5mH Single Pulse	506	mJ
T_J	Operation junction temperature	-55~150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-55~150	

➤ Thermal Resistance Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	30	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.0	

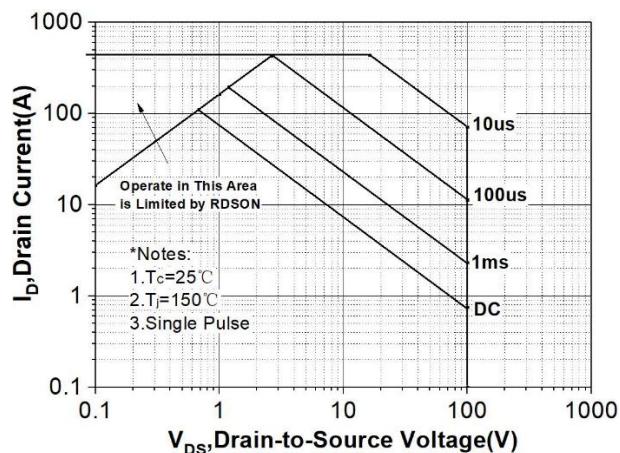
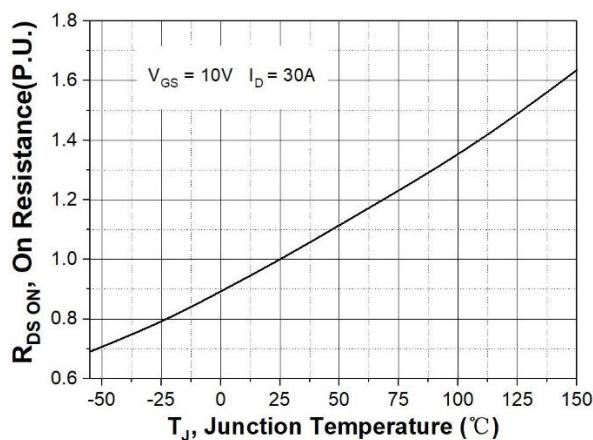
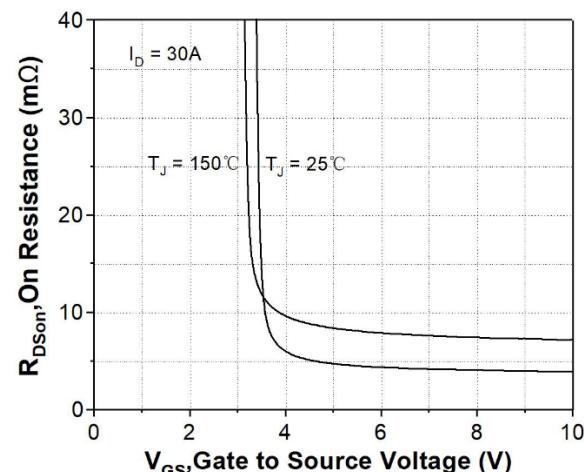
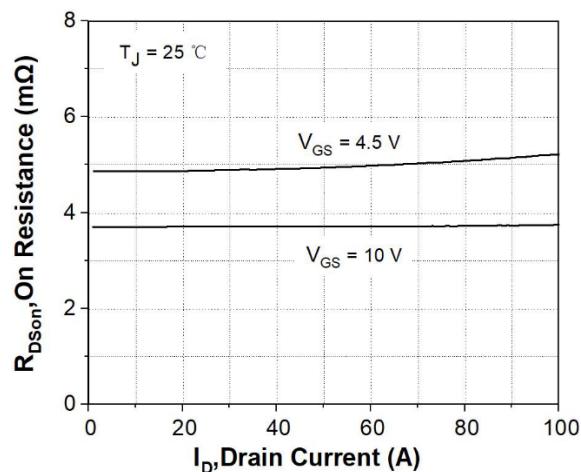
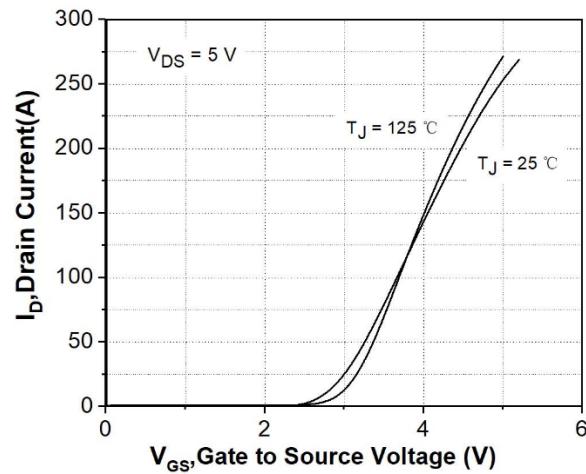
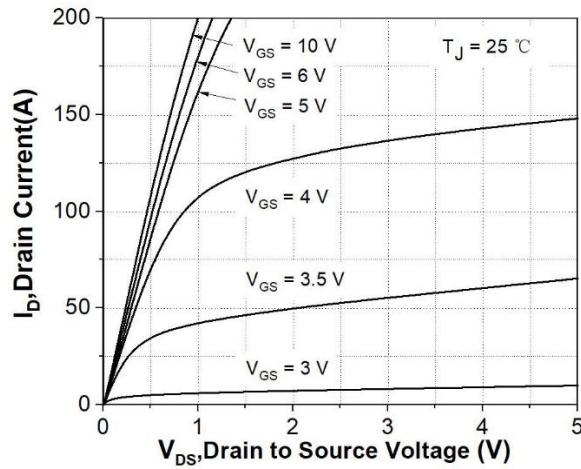
Note:

- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

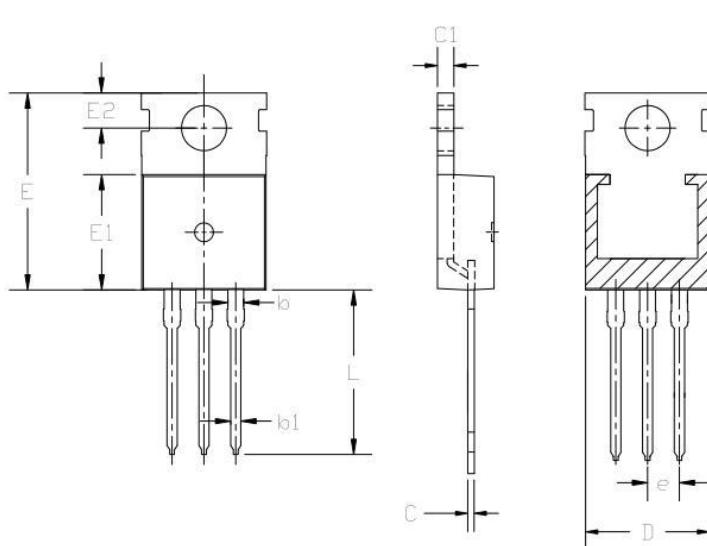
➤ Electrical Characteristics ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.4	2	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 30A$		3.7	5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 20A$		4.9	7.5	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$			1	μA
Gate-Source Leak Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
Transconductance	G_{FS}	$V_{DS} = 5V, I_D = 20A$		60		s
Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 20A$		0.8	1.3	V
Gate Resistance	R_G	$V_{DS} = 0V, f = 1MHz$		2.7		Ω
Input Capacitance	C_{ISS}	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1MHz$		4560		pF
Output Capacitance	C_{OSS}			674		
Reverse Transfer Capacitance	C_{RSS}			31		
Total Gate Charge	Q_G	$V_{GS} = 10V, V_{DS} = 50V,$ $I_D = 20A$		64		nC
Gate to Source Charge	Q_{GS}			15		
Gate to Drain Charge	Q_{GD}			11		
Turn-on Delay Time	$T_{D(ON)}$	$V_{GS} = 10V, V_{DS} = 50V,$ $R_L = 2.5\Omega, R_G = 3\Omega$		22		ns
Rise Time	T_r			27		
Turn-off Delay Time	$T_{D(OFF)}$			66		
Fall Time	T_f			73		
Diode Recovery Time	T_{rr}	$I_F=20A, di/dt=100A/us$		50		ns
Diode Recovery Charge	Q_{rr}	$I_F=20A, di/dt=100A/us$		110		nC

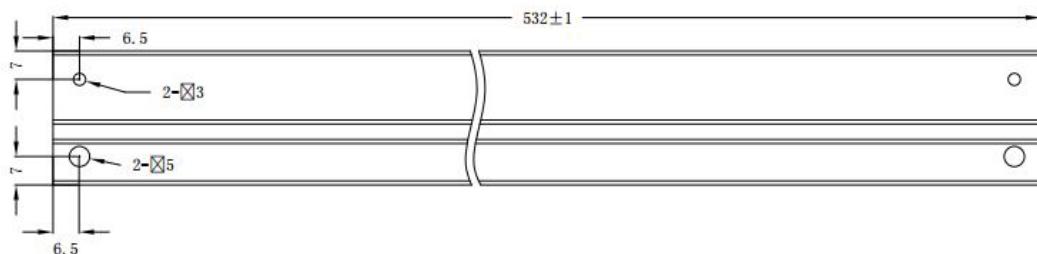
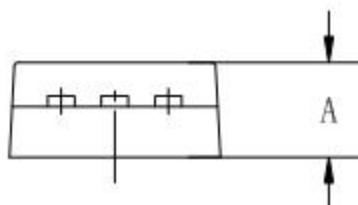
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



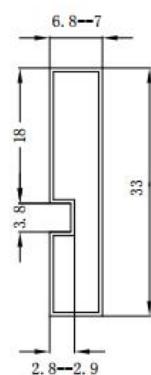
➤ Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.40	--	4.60
b	1.20	--	1.36
b ₁	0.70	--	0.90
C	0.48	--	0.53
C ₁	1.28	--	1.32
D	9.80	10.00	10.20
E	15.20	15.45	15.75
E ₁	9.00	9.20	9.40
E ₂	2.60	--	2.90
e	--	2.54	--
L	13.00	--	13.40



T=0.5 ± 0.1



技术要求:

- 材料: 透明PVC
- 表面电阻: 10E5~10E10 OHMS/SQ
- 未注尺寸公差±0.3
- 黑色钉子由厂家出货时塞于左端

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