



SSC8122GS9

N-Channel Enhancement Mode MOSFET

➤ Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D	ESD
20V	±8V	215mΩ@4V5	1A	2K
		260mΩ@2V5		
		310mΩ@1V8		

➤ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

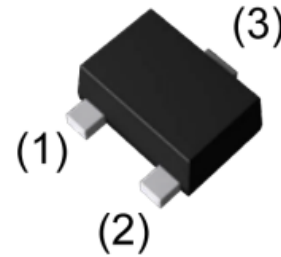
➤ Applications

- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones

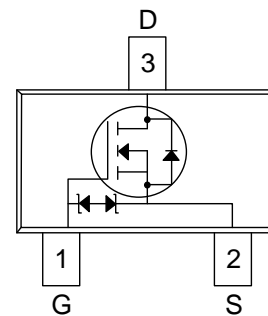
➤ Ordering Information

Device	Package	Shipping
SSC8122GS9	SOT-723	8000/Reel

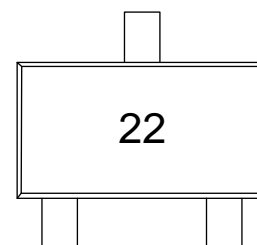
➤ Pin configuration



SOT-723



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	± 8	V
I_D	Continuous Drain Current ^a		A
I_{DM}	Pulsed Drain Current ^b	2.5	A
P_D	Power Dissipation ^c	0.3	W
P_{DSM}	Power Dissipation ^a	0.17	W
T_J	Operation junction temperature	-55~150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-55~150	$^\circ\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	735	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	416	$^\circ\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

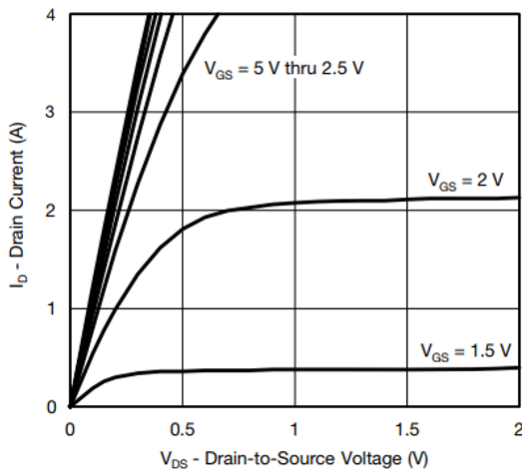


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

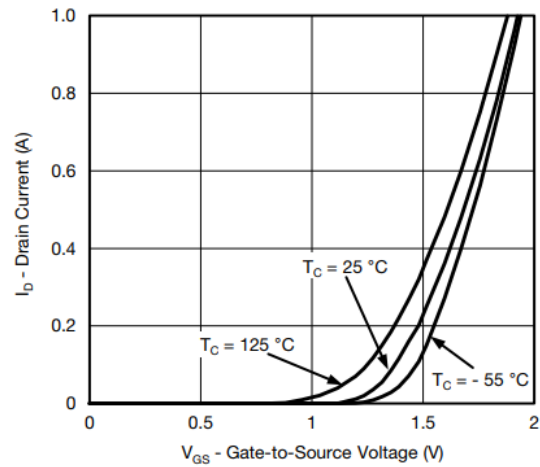
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	0.5	0.7	1	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5V, I _D = 0.5A		215	400	mΩ
		V _{GS} = 2.5V, I _D = 0.5A		260	500	
		V _{GS} = 1.8V, I _D = 0.35A		310	800	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±8V, V _{DS} = 0V			±10	μA
Transconductance	G _{FS}	V _{DS} = 10V, I _D = 0.4A		1		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 0.35A			1.2	V
Input Capacitance	C _{ISS}	V _{DS} = 10V, V _{GS} = 0V, f = 100kHz		86		pF
Output Capacitance	C _{OSS}			16		
Reverse Transfer Capacitance	C _{RSS}			8		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = 4.5V, R _G = 6Ω		22		ns
Turn-off Delay Time	T _{D(OFF)}	V _{DD} = 10V, I _D = 0.45A		36		



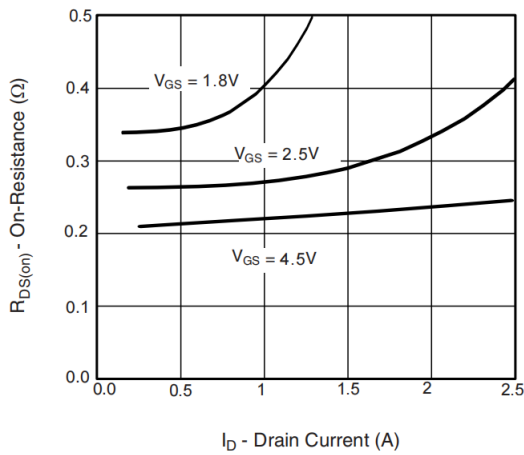
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



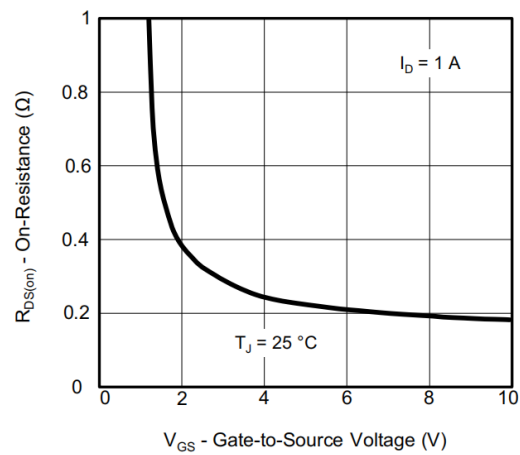
Output Characteristics



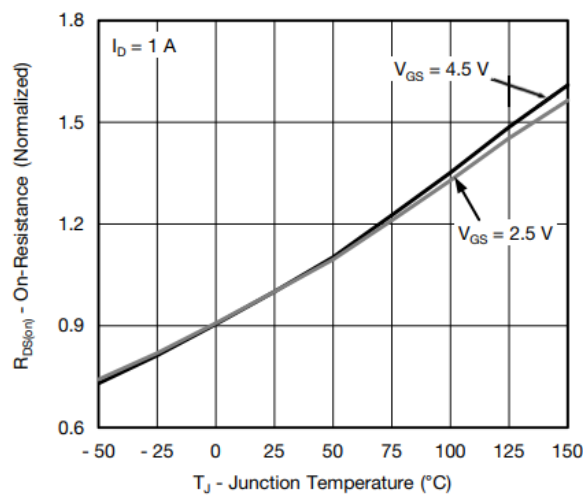
Transfer Characteristics



On-Resistance vs. Drain Current and Gate Voltage

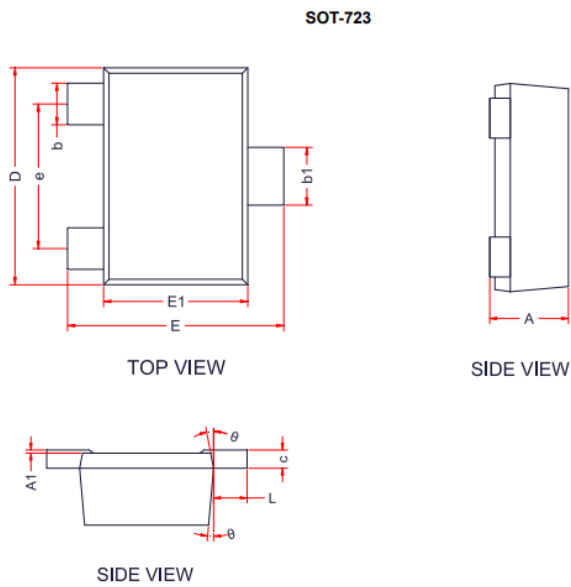


On-Resistance vs. Gate-to-Source Voltage



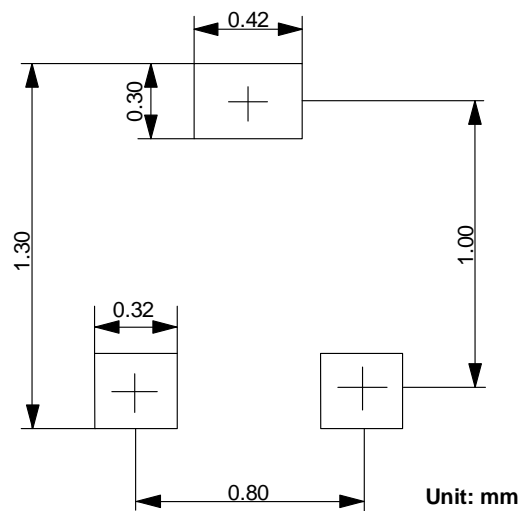
On-Resistance vs. Junction Temperature

➤ Package Information

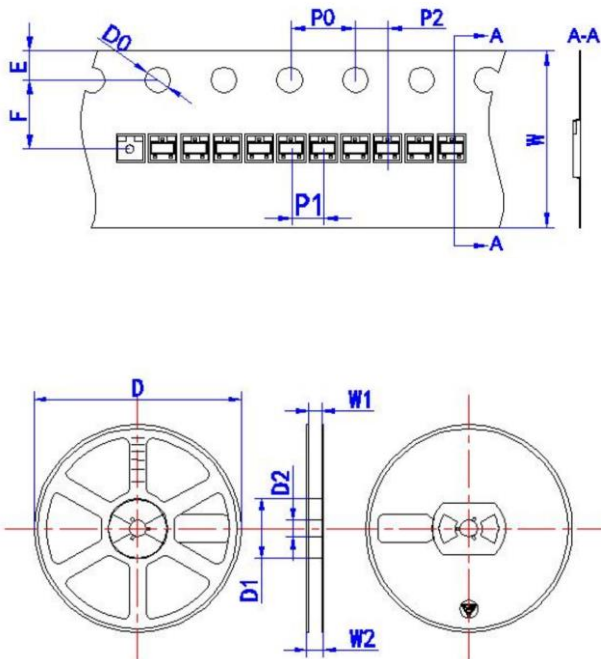


DIM	Millimeters		
	Min.	Typ.	Max.
A	0.43	-	0.55
A1	0.00	-	0.05
b1	0.27		0.37
b	0.17	-	0.27
c	0.08	0.13	0.18
D	1.15	1.20	1.25
E	1.15	1.20	1.25
E1	0.75	0.8	0.85
e	0.80Ref.		
L	0.15	0.2	0.25
θ	7°Ref.		

➤ Suggested Pad Layout



➤ Tape & Reel specification



DIM	Dimension in Millimeters
Tape	
D0	1.50+0.10/-0.00
E	1.75±0.10
F	3.50±0.10
P0	4.00±0.10
P1	2.00±0.10
P2	2.00±0.10
W	8.00+0.3/-0.1
Reel	
D	178.0±2.00
D1	54.40±1.00
D2	13.00±1.00
W1	9.50±1.00
W2	12.30±1.00

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