SSC8033GS1

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-30V	±20V	41mR@-10V	-6A
		56mR@-4V5	

➢ Description

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V-25V) such as load switch and battery protection.

➢ Applications

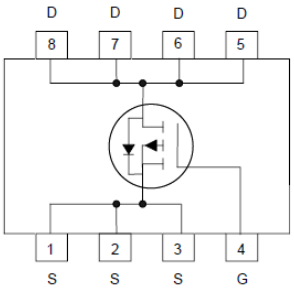
- Load Switch
- TFT panel power switch
- DCDC conversion

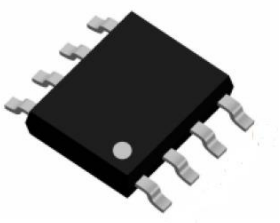
➢ Ordering Information

Device	Package	Shipping
SSC8033GS1	SOP8	2500/Reel

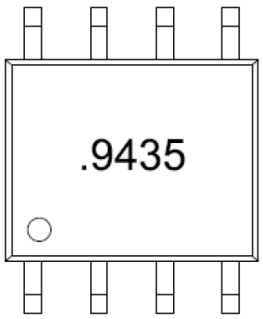
➢ Pin configuration

Top view





SOP8



Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-30	V
V_{GSS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current [a]	-6	A
I_{DM}	Pulsed Drain Current [b]	-25	A
P_D	Power Dissipation [c]	2.4	W
P_{DSM}	Power Dissipation [a]	1.3	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		100	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		55	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

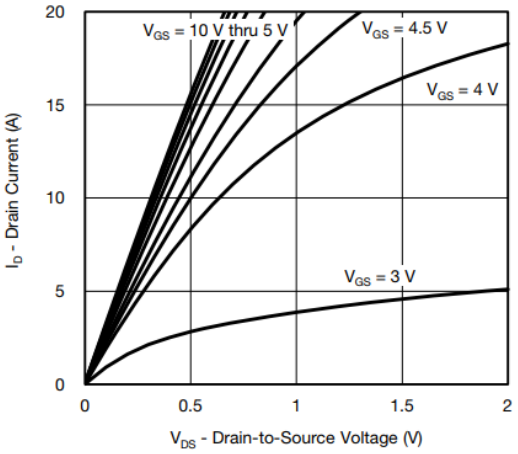
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

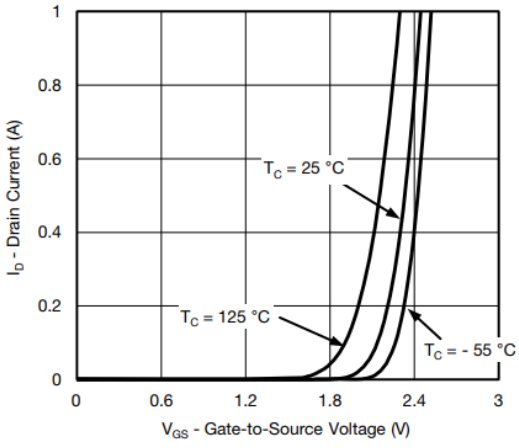
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=-250uA	-1	-1.5	-3	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-10V,ID=-4.5A		41	60	mR
		VGS=-4.5V,ID=-2A		56	96	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±20V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V,ID=-6A		12		S
V_{SD}	Forward Voltage	VGS=0V,IS=-1A		-0.8	-1.6	V
Ciss	Input Capacitance	VDS=-15V, VGS=0V, f=1MHz		550		pF
Coss	Output Capacitance			60		
Crss	Reverse Transfer Capacitance			50		
$T_{D(ON)}$	Turn-on delay time	VGS=-10V, VDS=-15V, RL=2.5R, RG=3R		8.6		ns
Tr	Rise time			7.4		
$T_{D(OFF)}$	Turn-off delay time			28.2		
Tf	Fall time			16		

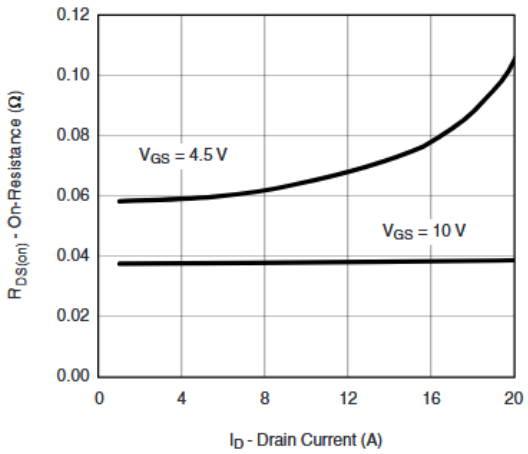
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



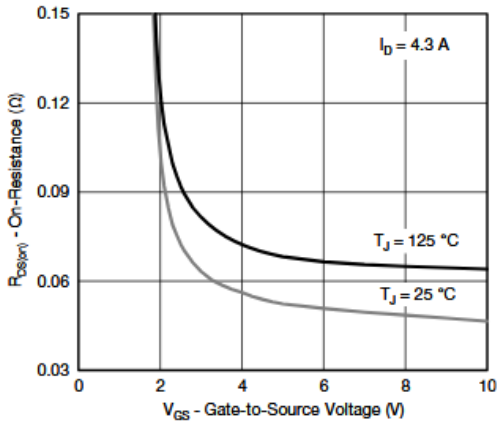
Output Characteristics



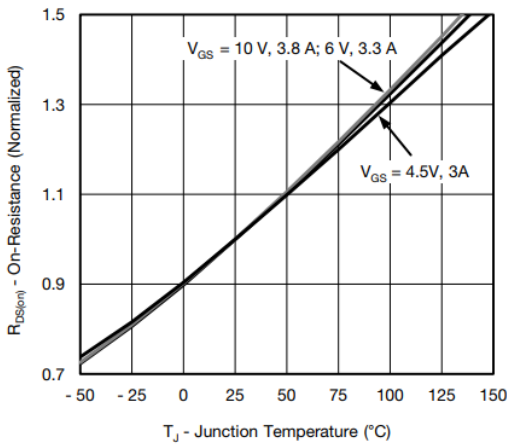
Transfer Characteristics



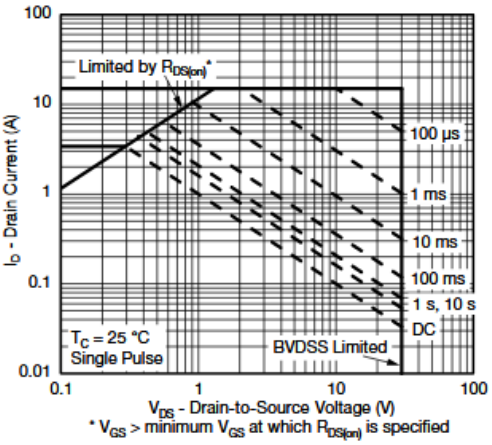
On-Resistance vs. Drain Current



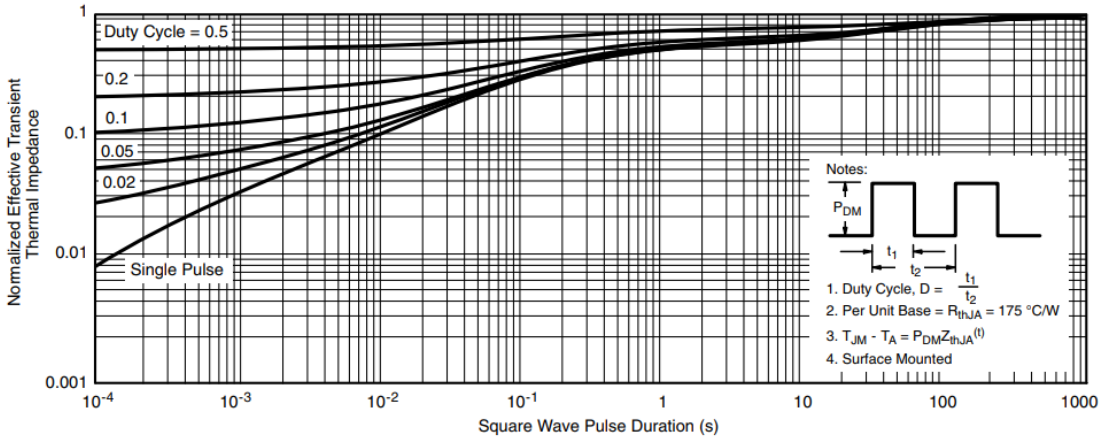
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

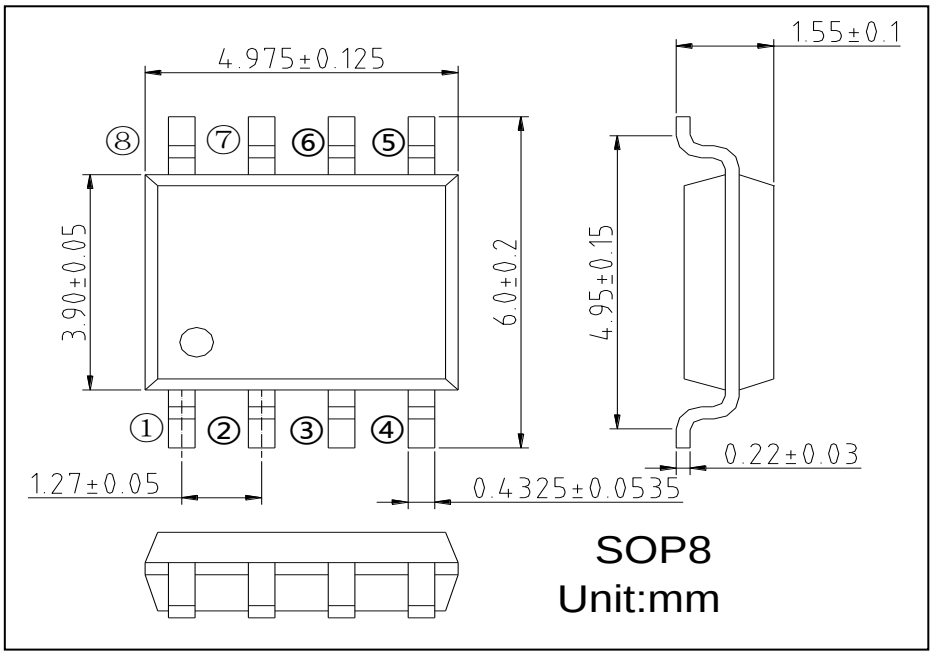


Safe Operating Area, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

➢ Package Information



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