SSC8126GN1

N-Channel Enhancement Mode MOSFET with ESD protection

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$	I_D	ESD
20V	±8V	210mΩ@4V5	1A	2K
		260mΩ@2V5		
		330mΩ@1V8		

➢ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

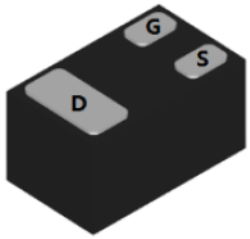
➢ Applications

- Load Switch
- Portable Devices

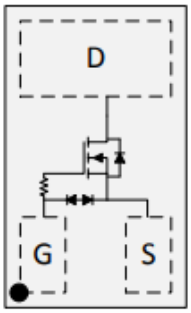
➢ Ordering Information

Device	Package	Shipping
SSC8126GN1	DFN1006-3L	10000/Reel

➢ Pin configuration



DFN1006-3L (Bottom View)



Pin Configuration (Top View)

Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Gate-to-Source Voltage	V_{GSS}	±8	V
Continuous Drain Current [a]	I_D	1	A
Pulsed Drain Current [b]	I_{DM}	3	A
Power Dissipation [c]	P_D	0.32	W
Power Dissipation [a]	P_{DSM}	0.18	W
Operation junction temperature, Storage temperature range	T_J, T_{STG}	-55 to 150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	690	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	379	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤10s thermal resistance rating.

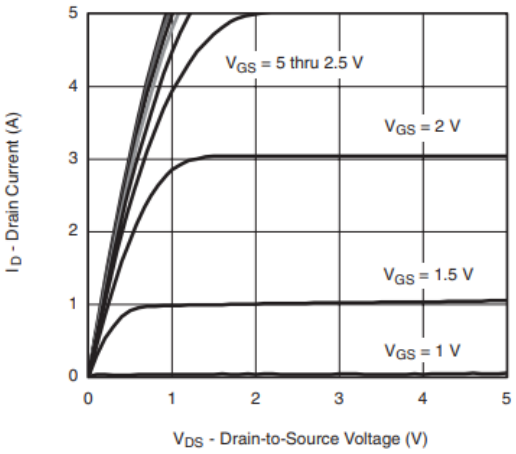
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

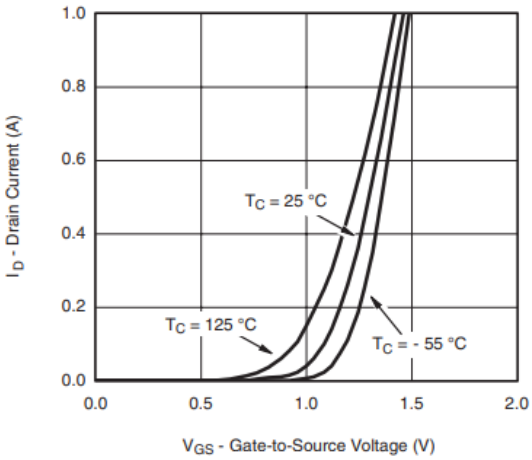
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.5	0.68	1	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 0.5A		210	350	mΩ
		V_{GS} = 2.5V, I_D = 0.35A		260	420	
		V_{GS} = 1.8V, I_D = 0.35A		330	500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0V			±10	μA
Transconductance	G_{FS}	V_{DS} = 5V, I_D = 0.5A		2		s
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 0.5A		0.7	1.3	V
Input Capacitance	C_{ISS}	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		66		pF
Output Capacitance	C_{OSS}			18		
Reverse Transfer Capacitance	C_{RSS}			9		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = 4.5V, V_{DS} = 10V, R_G = 6Ω, I_D = 0.6A		20		ns
Rise Time	T_r			13		
Turn-off Delay Time	$T_{D(OFF)}$			40		
Fall Time	T_f			12		

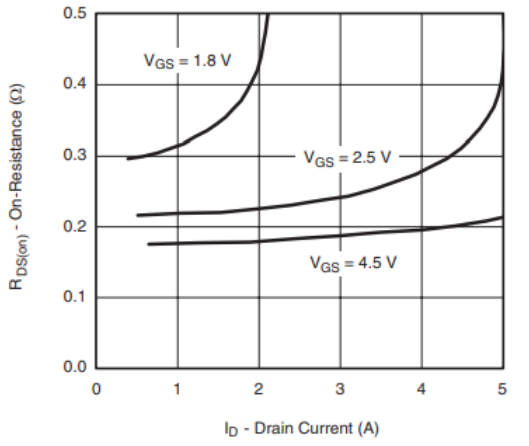
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



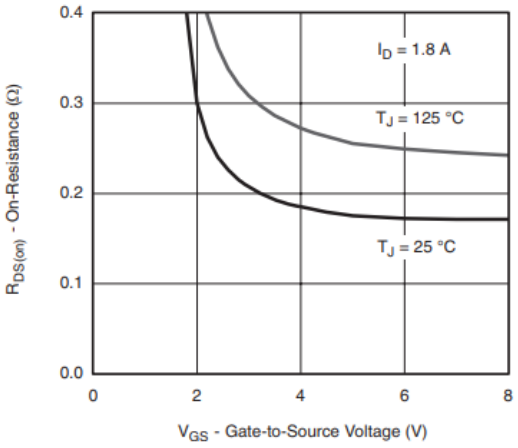
Output Characteristics



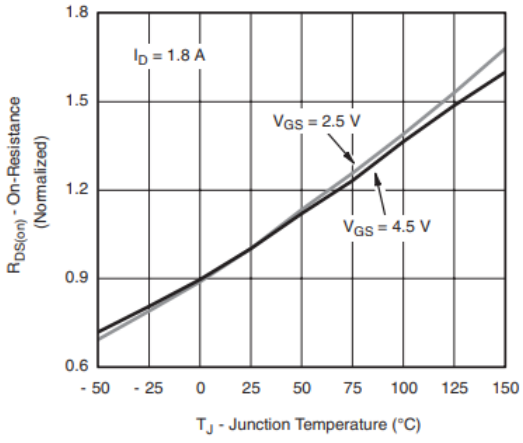
Transfer Characteristics



On-Resistance vs. Drain Current and Gate Voltage



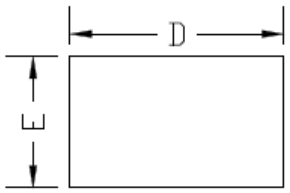
On-Resistance vs. Gate-to-Source Voltage



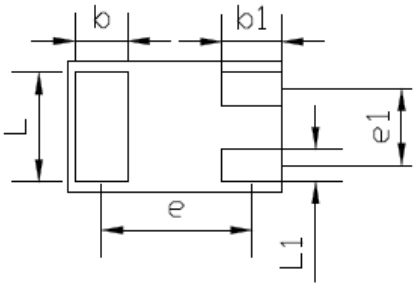
On-Resistance vs. Junction Temperature

➢ Package Information

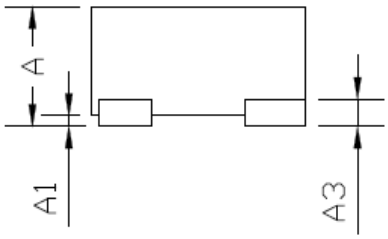
POD



TOP VIEW



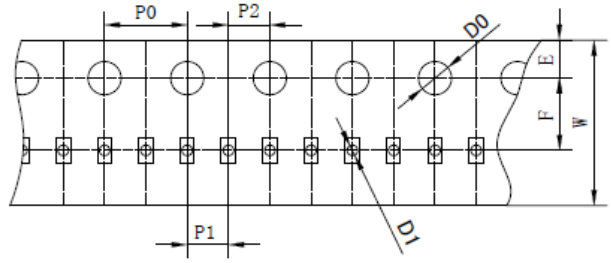
BOTTOM VIEW

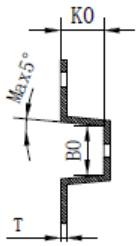


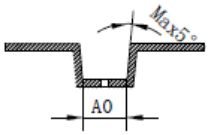
SIDE VIEW

COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	–	0.50
A1	0.00	–	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

Tape Data



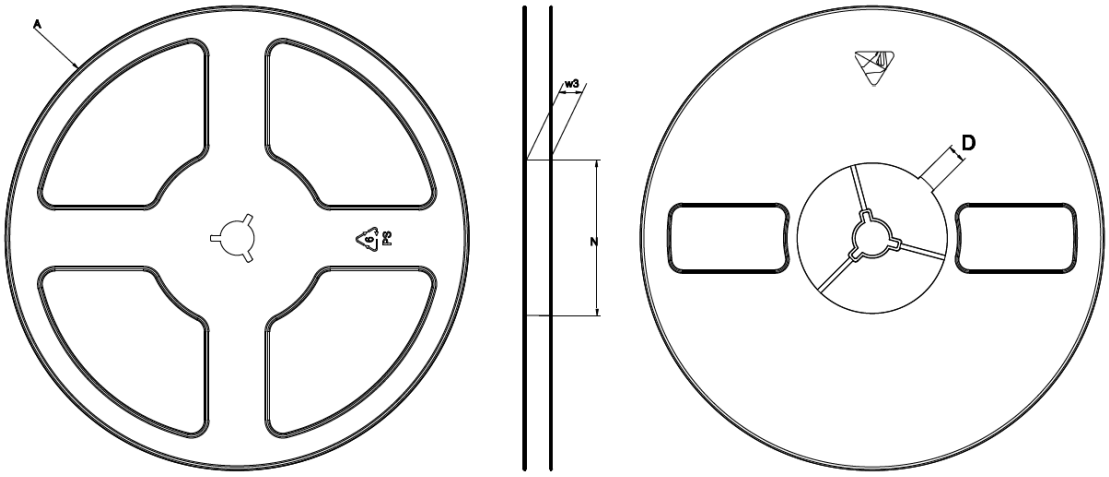


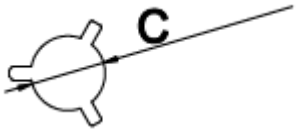


SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	0.69±0.05	1.15±0.05	0.60±0.05	4.00±0.10	2.00±0.05	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.18±0.03	1.75±0.10	3.50±0.05	1.55±0.05	0.50±0.05	8.00 $^{+0.3}_{-0.1}$

NOTE:
1. 材料：黑色防静电材料；
2. 10个链孔的累积公差不能超过±0.2
3. 尺寸符合EIA-481-E的要求。

Reel Data





材质说明：该产品用料为 PS

TYPE	A	N	C	D	w3
8MM	Ø178 +1 -1	Ø60 +1 -1	Ø13,3 +0,3 -0,3	7,5±0,5	9±0.3

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