



SSC8027GN1

P-Channel Enhancement Mode MOSFET

➤ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-20V	$\pm 8V$	100m Ω @-4.5V	-2A
		125m Ω @-2.5V	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

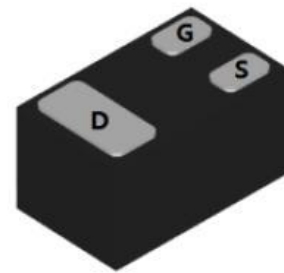
➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion

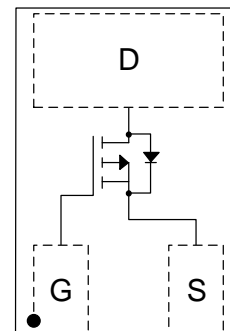
➤ Ordering Information

Device	Package	Shipping
SSC8027GN1	DFN1006-3L	10000/Reel

➤ Pin configuration



DFN1006-3L (Bottom View)



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 8	V
I_{D}	Continuous Drain Current ^a	-2	A
I_{DM}	Pulsed Drain Current ^b	-8	A
P_{D}	Power Dissipation ^a	0.8	W
T_{J}	Operation junction temperature	-55~150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55~150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Maximum	Unit
$R_{\theta\text{JA}}$	Junction-to-Ambient Thermal Resistance ^a	166	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta\text{JA}}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.

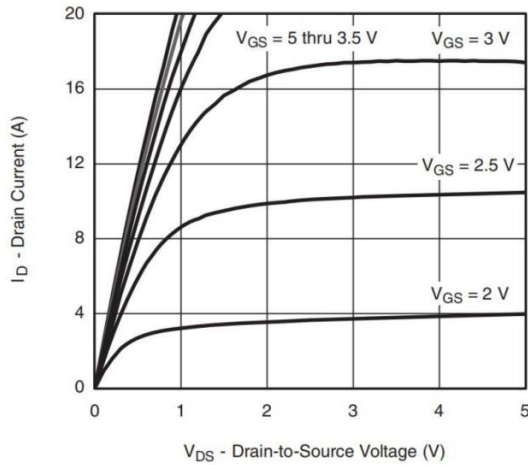


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

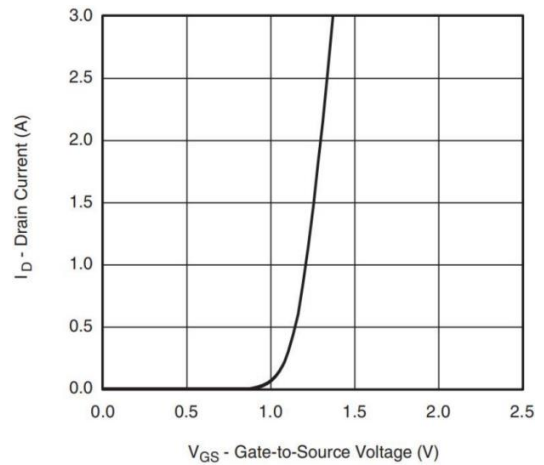
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-0.45	-0.8	-1.2	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -0.45A		100	160	mΩ
		V _{GS} = -2.5V, I _D = -0.35A		125	240	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20V, V _{GS} = 0V			-1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±8V, V _{DS} = 0V			±100	nA
Transconductance	G _{FS}	V _{DS} = -5V, I _D = -1A		7		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -1A	-0.5	-0.7	-1.2	V
Input Capacitance	C _{ISS}	V _{DS} = -6V, V _{GS} = 0V, f = 1MHz		370		pF
Output Capacitance	C _{OSS}			200		
Reverse Transfer Capacitance	C _{RSS}			80		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = -6V, V _{GEN} = -4.5V, R _L = 6Ω, R _G = 6Ω, I _D = -1A		16		ns
Rise Time	T _r			10		
Turn-off Delay Time	T _{D(OFF)}			45		
Fall Time	T _f			11		



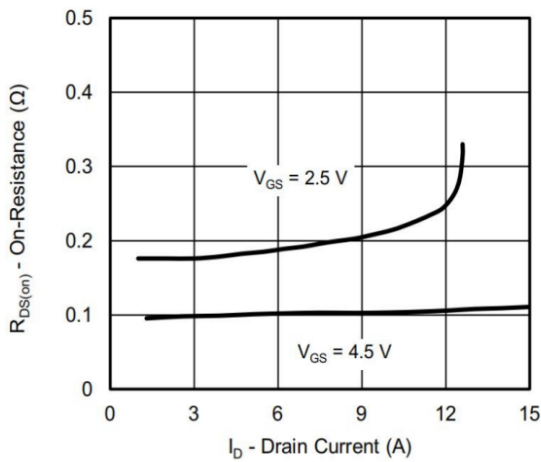
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



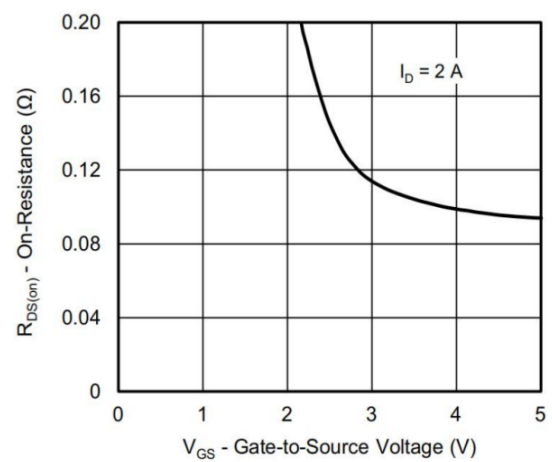
Output Characteristics



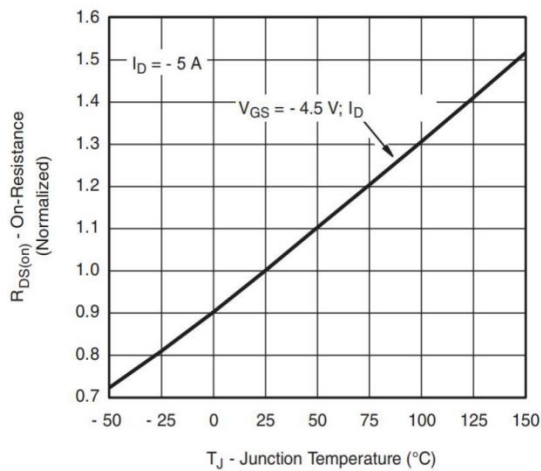
Transfer Characteristics



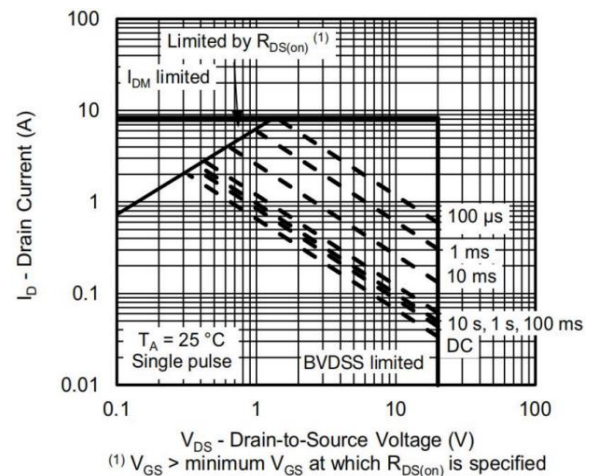
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage



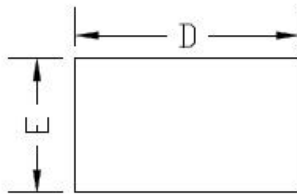
On-Resistance vs. Junction Temperature



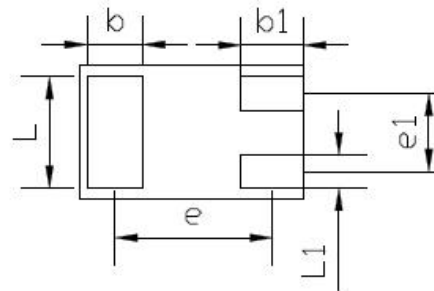
(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

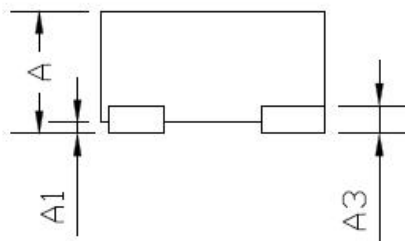
➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	-	0.50
A1	0.00	-	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

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