SSC8125GS6

P-Channel Enhancement Mode MOSFET with ESD Protection

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
-20V	±8V	36mR @-4.5V	-4A	3kV
		45mR @-2.5V		
		57mR@-1.8V		

➢ Description

This device uses advanced trench technology to provide excellent RDSON, low gate charge and operation with gate voltages as low as 1.5V and it is protected from ESD. These features make it suitable for use as a load switch or in PWM applications.

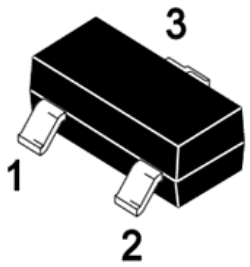
➢ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

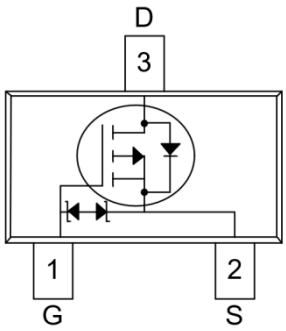
➢ Ordering Information

Device	Package	Shipping
SSC8125GS6	SOT-23	3000/Reel

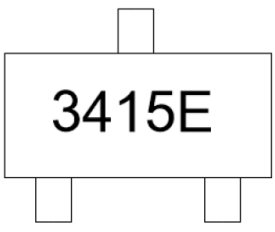
➢ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current [a]	-4	A
I_{DM}	Pulsed Drain Current [b]	-20	A
P_D	Power Dissipation [c]	0.9	W
P_{DSM}	Power Dissipation [a]	0.45	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance		280	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		140	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

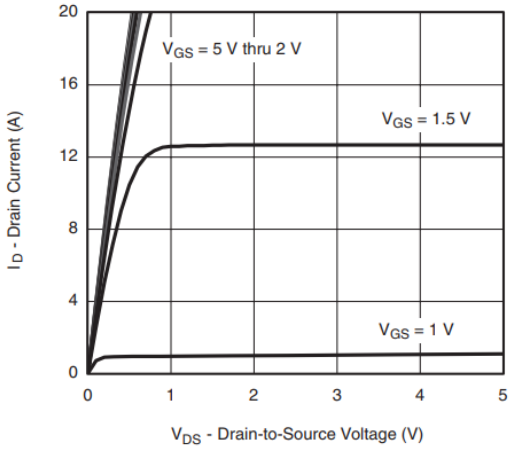
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

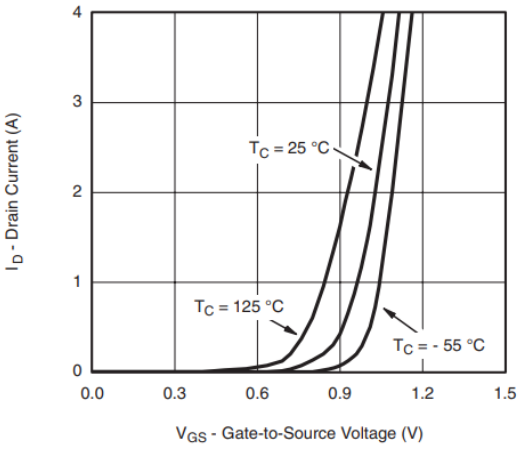
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.4	-0.6	-0.9	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V , I_D=-4A		36	41	mΩ
		V_{GS}=-2.5V , I_D=-3A		45	52	
		V_{GS}=-1.8V , I_D=-2A		57	62	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±10	uA
Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-1.6A		-0.7	-1.3	V
Input Capacitance	C_{ISS}	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		418		pF
Output Capacitance	C_{OSS}			136		
Reverse Transfer Capacitance	C_{RSS}			56		
Turn-on Delay Time	$T_{D(ON)}$	VGS=-5V, VDS=-10V, RL=1.5R, RG=3R		18		ns
Rise Time	T_r			12		
Turn-off Delay Time	$T_{D(OFF)}$			70		
Fall Time	T_f			25		

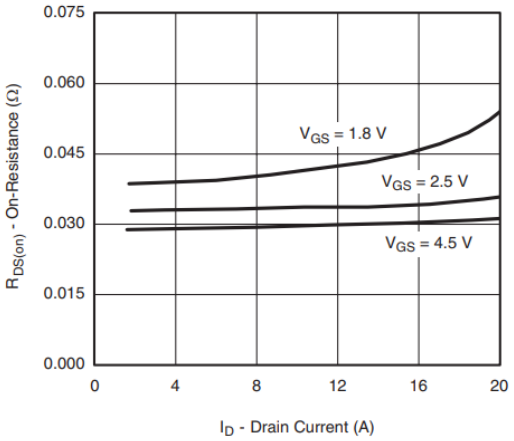
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



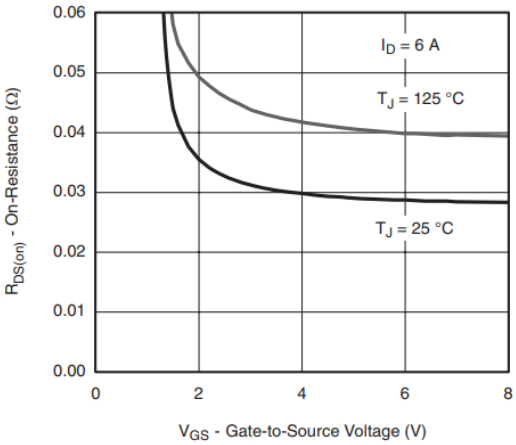
Output Characteristics



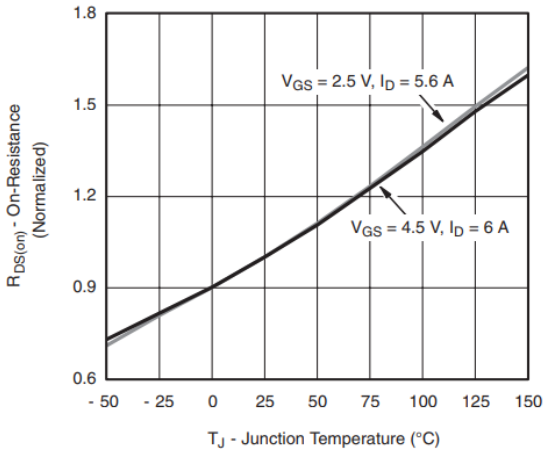
Transfer Characteristics



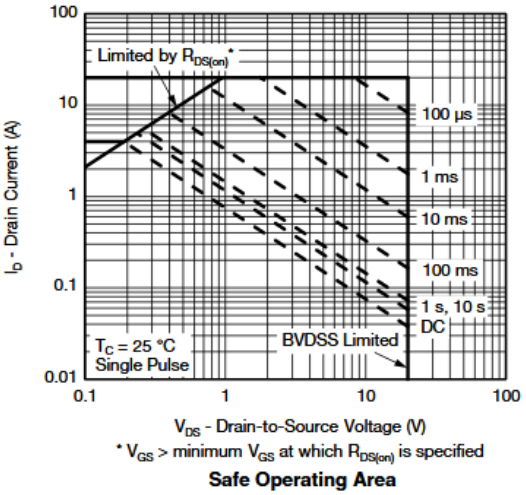
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

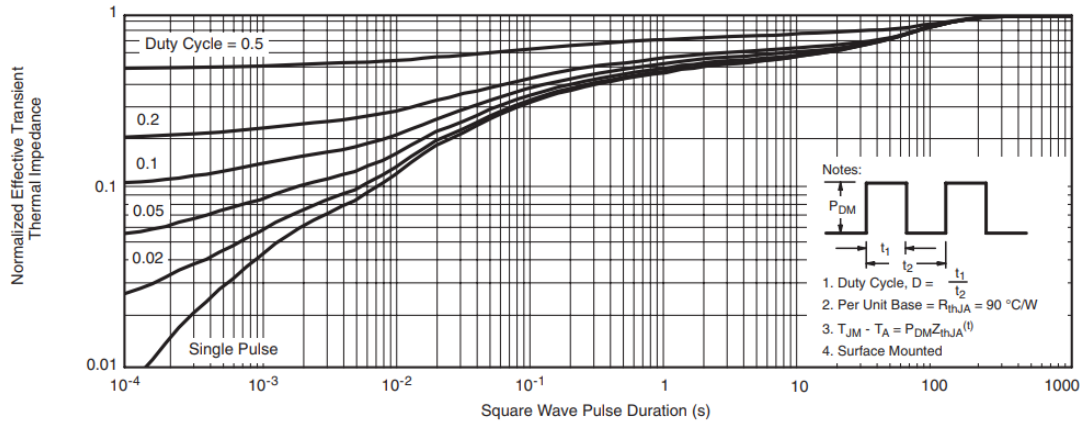


On-Resistance vs. Junction Temperature



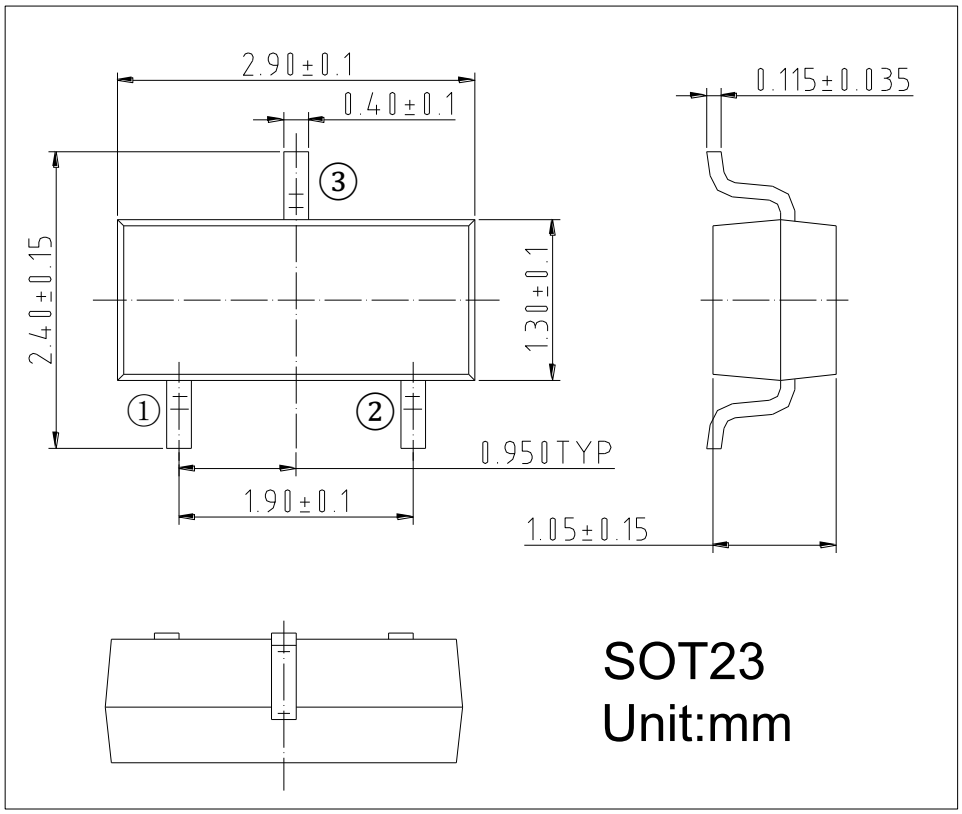
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

➢ Package Information



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